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RM-6503

B. E. II (Sem. IV) (Ele.) Examination

May / June – 2010

Electronics Circuit - II

Time : **3** Hours] [Total Marks : **100**

Instruction :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 2 (Sem. 4) (Ele.)**

Name of the Subject :

☛ **Electronics Circuit - 2**

☛ Subject Code No. : **6 5 0 3** ☛ Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

SECTION - I

(2) Attempt **all** questions.

(3) Assume suitable data whenever **necessary**.

(4) Figures to **right** indicate full marks.

(5) Use of scientific calculator (fx-82 100 W MS-82 F-100MS) is permitted.

1 (a) Answer the following questions :

(i) The Darlington amplifier provides _____ i/p impedance and _____ current gain. (High-High, Low-High) **1**

(ii) A differential amplifier has differential made gain of 100 and common mode gain of 0.01. Calculate its CMRR in dB. **2**

(iii) What is the difference between oscillator and amplifier? **1**

(iv) In RC phase shift oscillator each RC n/w provides _____° phase shift (0°, 30°, 60°, 180°). 1

(v) For Hartley oscillator fo = _____. 1

(vi) For colpits oscillator fo = _____. 1

(vii) Draw the current shunt P voltage shunt topology. 2

(viii) For ideal amplifier Ri = _____ (0, ∞) 1

(b) Draw cascade (CE-CB) amplifier. 2

(c) In **fig. 1**, the transistors are identical with h_{fe} = 100, $h_{re} = h_{oe} = 0$. 8

(i) Find IE_{Q1}, IE_{Q2}, assuming the dc common made voltage is negligible.

(ii) Find Ad, Aa, CMRR.

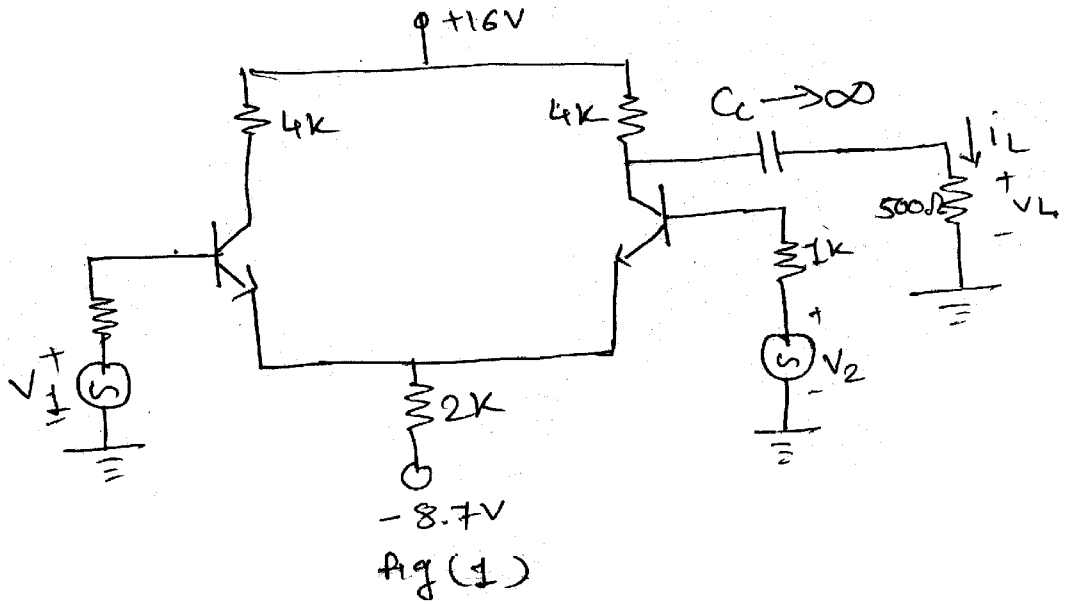

fig (1)

2 (a) In the two stage feedback amplifier shown in **fig. 2** the transistors are identical and have the following parametesr: h_{fe} = 50, h_{ie} = 2k. Calculate 8

(i) $A_{if} = \frac{l_0}{l_s}$ (ii) $R_{if} = \frac{V_i}{i_0}$ (iii) $A_{if'} = \frac{i_0}{i_i}$

(iv) $A_{vf} = \frac{V_0}{V_s}$ where $V_s = i_s R_s$.

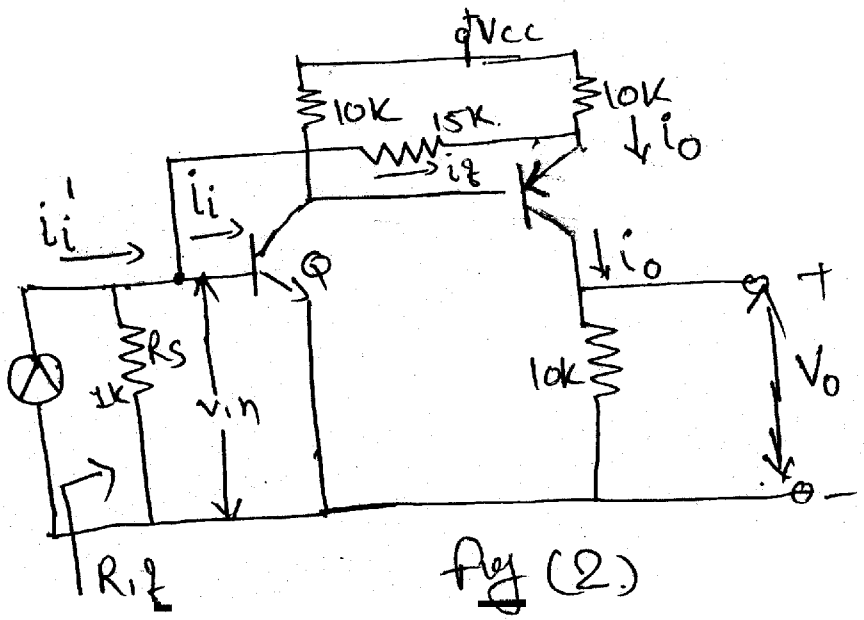

Fig (2)

(b) List the advantages and disadvantages of negative feedback. **7**

OR

2 (a) For the transistor feedback amplifier stage shown in **fig. 3** $h_{fe} = 100$, $h_{ie} = 1k$, determine with emitter resistor by passed by C_e : **10**

(i) $R_{MF} = \frac{V_0}{i_s}$ where $i_s = \frac{V_s}{R_s}$

(ii) $A_{vf} = \frac{V_0}{V_s}$

(iii) R_{if}

(iv) R_{of} '

(v) Repecet the four

Preceding calculations if emitter resistance is unbypassed.

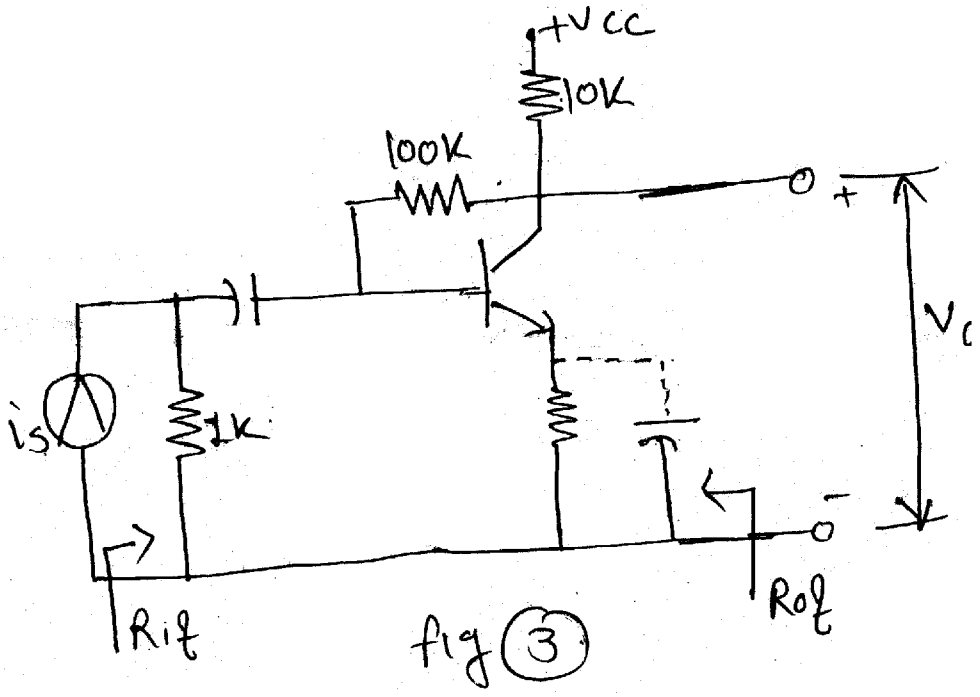

fig (3)

(b) For voltage series feedback obtain the expressions for input resistance Ri f. **5**

3 (a) Explain Wein bridge oscillator and derive the frequency of oscillation. **8**

(b) Explain Hartley oscillator and derive the frequency of oscillation. **7**

OR

3 (a) Explain RC phase shift oscillator and derive the frequency of oscillation. **8**

(b) Explain Colpitt's oscillator and derive the frequency of oscillation. **7**

SECTION - II

4 (a) Do as directed : **10**

(i) Explain what do you mean by frequency response of an amplifier.

(ii) Define pulse input.

(iii) What capacitors affect the gain at high frequency ?

(iv) Explain clipping.

(v) Clamping circuit is known as DC restorer circuit. State true or false.

(vi) MOSFET stands for _____.

(vii) After pinch off voltage _____ becomes constant (current, voltage)

(viii) Draw the symbol of P - channel JFET.

(ix) For N-channel JFET the gain to source voltage is positive. State true or false.

(x) Draw the frequency response of RC coupled amplifier.

(b) (i) Draw and explain construction and transfer characteristic of P-channel JFET. **6**

(ii) Explain ramp input in high pass RC circuit. **4**

5 (a) For the CE amplifier in the **fig. 4** calculate the mid-frequency voltage gain and lower 3-dB point. The circuit details are R_s = 600 Ω, R_L=5 K Ω,R_E=1kΩ, V_{CC}=12V R_1 = 15 kΩ R_2 = 2.2 kΩ, C_e = 50 μF. Draw the bode plot h_{ie} = 1kΩ, h_{fe} = 50. **7**

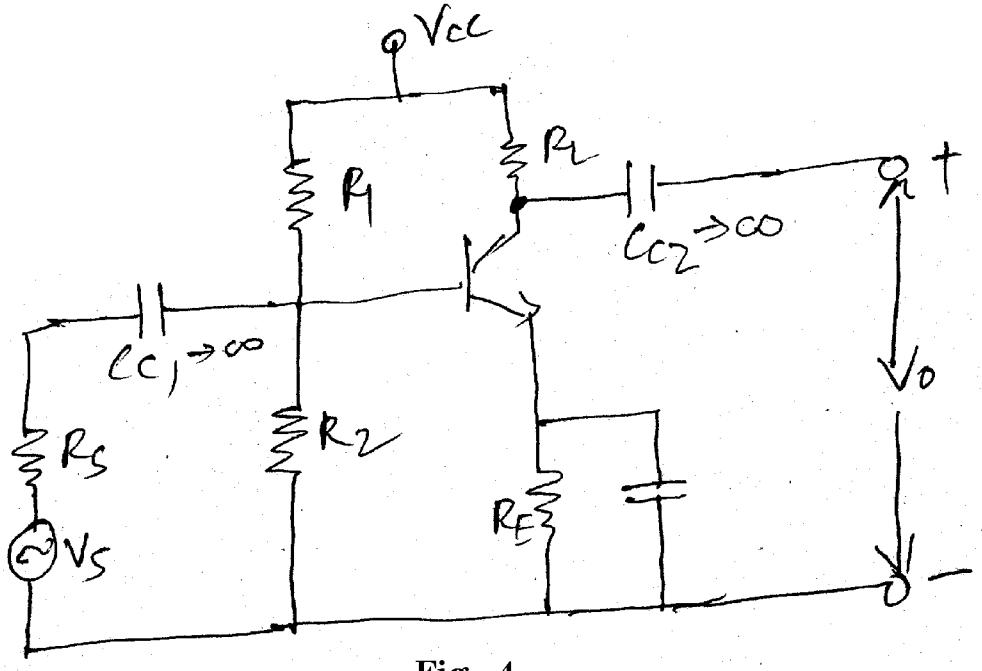

Fig. 4

(b) Obtain transfer characteristic for **fig. 5** below. Assume ideal diodes. Sketch the output if V_i = 150 sinwt. 7

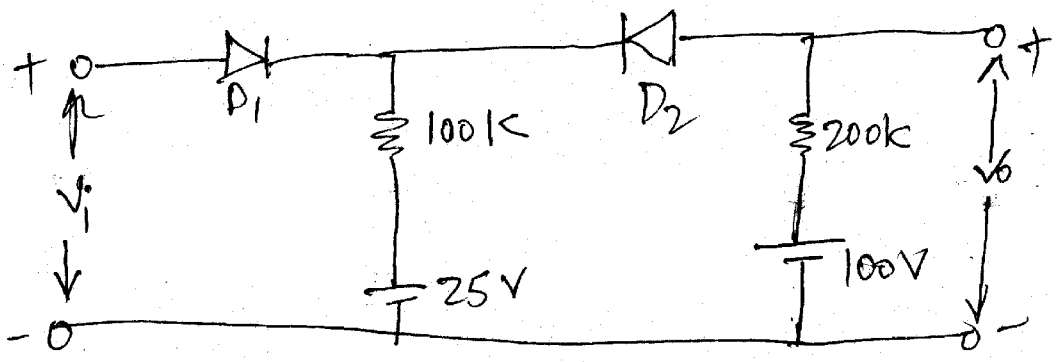

Fig. 5

OR

5 (a) Draw and explain the response of square wave to the RC low pass circuit. 7

(b) Obtain transfer characteristic for the circuit shown below. Assume ideal diodes. Sketch output for V_i = 40 sinwt. 8

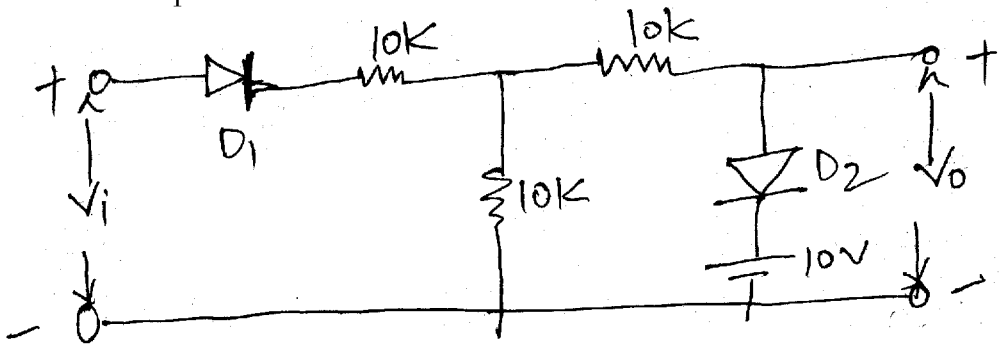

Fig. 6

6 Attempt any **three** : 15

(i) State and prove clamping circuit theorem.

(ii) The amplifier shown in the figure below is to have lower 3dB frequency at 20Hz. Select CC_1 CC_2 and C_e to meet specifications for BJT h_{fe} = 100, h_{ie} = 1 k Ω.

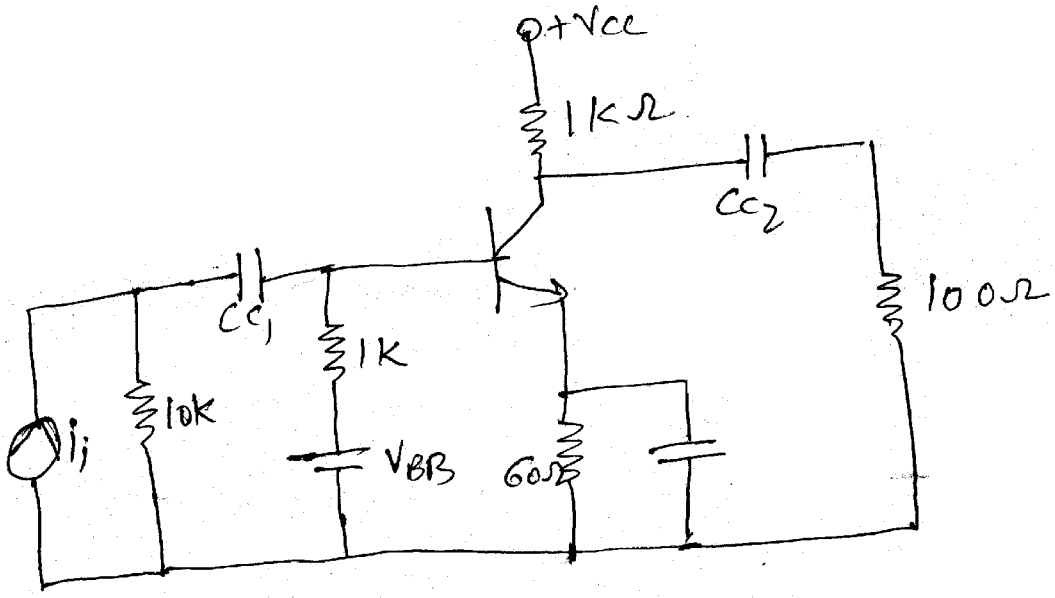

Fig. 7

(iii) Write short note on comparators.

(iv) Explain Enhancement MOSFET.
